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What is claimed is:

1. A method for fabricating a semiconductor device, comprising:

preparing a substrate having a silicon region;

causing the silicon region to be amorphous by an ion implantation;

heating the substrate having the amorphous silicon region at a predetermined temperature;

forming a metallic layer on the amorphous silicon region, wherein the metallic layer has a first thickness;

forming a protective layer on the metallic layer, wherein the protective layer protects the metallic layer from a surround atmosphere, wherein the protective layer has a second thickness thicker than the first thickness;

forming a metallic silicide layer in an interface between the amorphous silicon region and the metallic layer by a heat treatment, wherein the metallic silicide layer is comprised of metal in the metallic layer and silicon in the amorphous silicon region.

2. The method according to claim 1, wherein argon ions are implanted into

the silicon region by the ion implantation.

3. The method according to claim 1, wherein the predetermined temperature is a temperature of from 200℃ to 400℃.

4. The method according to claim 1, wherein the metallic layer is formed on the amorphous silicon region by a long throw sputtering method or a collimate sputtering method.

5. The method according to claim 1, wherein the metallic layer is comprised of titanium, cobalt or nickel.

6. The method according to claim 1, wherein a depth of the silicon region is larger than the first thickness of the metallic layer.

7. The method according to claim 1, wherein the protective layer is comprised of titanium-nitride or tungsten.

8. The method according to claim 1, wherein the first thickness of the metallic layer is equal to or less than 15nm.

9. The method according to claim 1, wherein the second thickness of the protective layer is equal to or more than 30nm.

10. The method according to claim 1, wherein a source region and a drain region of a MOS transistor are formed in the silicon region, wherein the metallic silicide layer is formed in the source and drain regions.

11. The method according to claim 1, wherein the substrate has a silicon on insulator structure which has a single silicon layer formed on an insulating film.

12. A method for fabricating a semiconductor device, comprising:

preparing a SOI substrate having a single silicon region formed on an insulating film;

heating the SOI substrate at a temperature of from 200℃ to 400℃;

forming a metallic layer on the single silicon region of the SOI substrate;

forming a protective layer on the metallic layer, wherein the protective layer protects the metallic layer from a surround atmosphere;

forming a metallic silicide layer in a surface of the silicon region by a heat treatment, wherein the metallic silicide layer is comprised of metal in the metallic layer and silicon in the amorphous silicon region.

13. The method according to claim 12, wherein the metallic layer has a first thickness, wherein the protective layer has a second thickness which is more than the first thickness of the metallic layer.

14. The method according to claim 12, wherein argon ions are implanted into the silicon region by an ion implantation before the step of heating the SOI substrate so as to form an amorphous silicon region in the silicon region.

15. The method according to claim 14, wherein the metallic layer is formed on the amorphous silicon region by a long throw sputtering method or a collimate sputtering method.

16. The method according to claim 15, wherein the metallic layer is comprised of titanium, cobalt or nickel.

17. The method according to claim 16, wherein the protective layer is comprised of titanium-nitride or tungsten.

18. The method according to claim 13, wherein a depth of the silicon region is larger than the first thickness of the metallic layer.

19. The method according to claim 13, wherein the first thickness of the

metallic layer is equal to or less than 15nm.

20. The method according to claim 19, wherein the second thickness of the protective layer is equal to or more than 30nm.